

AMENDMENTS TO THE CLAIMS

- 1 1. (Original) A current mirror, comprising:
2 a first leg comprising a reference current source operable to generate a reference
3 current;
4 a first mirror current leg comprising a first P-type CMOS transistor and a first N-
5 type transistor;
6 a second mirror current leg comprising a second P-type CMOS transistor and a
7 second N-type transistor;
8 a load leg comprising a third P-type transistor and a load; and
9 compensation circuitry operable to compensate for gate leakage in said
10 first, second and third P-type CMOS transistors.

- 1 2. (Original) The current source according to claim 1, wherein said
2 reference current is passed through an N-type CMOS transistor connected in a diode
3 configuration.

- 1 3. (Original) The current mirror according to claim 1, wherein said
2 compensation circuitry comprises first and second P-type compensation transistors.

- 1 4. (Currently Amended) The current mirror according to claim 3, wherein
2 said first compensation transistor is connected in a diode configuration and is operable to
3 sense and provide the a portion of the a copied reference current that is lost due to gate
4 current leakage of said first, second and third P-type CMOS transistors.

- 1 5. (Original) The current mirror according to claim 4, wherein said
2 second P-type compensation transistor generates a compensation current equal to the
3 portion of the copied reference current that is lost due to the gate current leakage of said
4 first, second and third P-type CMOS transistors.

- 1 6. (Original) The current mirror according to claim 5, wherein said load
2 comprises a charge pump circuit for a phase-locked loop.

1 7. (Original) The current mirror according to claim 5, wherein said
2 current mirror comprises at least three output current sources.

1 8. (Original) The current mirror according to claim 7, wherein current
2 mirror comprises a first sensing transistor in a diode configuration and at least three
3 compensation devices to compensate for gate current leakage in said first, second and
4 third P-type CMOS transistors.

1 9. (Original) The current mirror according to claim 8, wherein said
2 compensation devices comprise P-type CMOS transistors.

1 10. (Original) The current mirror according to claim 9, wherein said three
2 output current sources each comprise at least one P-type CMOS transistor and wherein
3 said compensation devices compensate for gate current leakage in said P-type CMOS
4 transistors.

1 11. (Currently Amended) A method of operating a current mirror circuit
2 having a reference leg, first and second mirror legs and a leg load each comprising at
3 least one P-type CMOS transistor and a lead leg, comprising:
4 generating a known reference current in said reference leg of said current mirror
5 circuit;
6 using said reference current to control the flow of current in said first and second
7 mirror legs and said load leg of said current mirror circuit;
8 compensating for gate current leakage in said P-type CMOS transistors in said
9 first and second mirror legs and the output load leg, thereby generating a
10 current flow in said load leg equal to the current flow in said reference leg.

1 12. (Original) The method according to claim 11, wherein said reference
2 current is passed through an N-type CMOS transistor connected in a diode configuration.

1 13. (Currently Amended) The method according to claim 12, wherein said
2 compensation ~~circuitry~~ comprises first and second P-type compensation transistors.

1 14. (Currently Amended) The method according to claim 13, wherein said
2 first compensation transistor senses and generates ~~the a~~ compensation current equal to the
3 sum of all ~~net~~ gate current leakage through the diode connection of the first P-type
4 CMOS transistor in the first mirror leg of said all P-type CMOS transistors.

1 15. (Currently Amended) The method according to claim 14, wherein said
2 second P-type compensation transistor copies the compensation current from the first P-
3 type compensation transistor and adds the compensation current to ~~the a~~ mismatched
4 output current.

1 16. (Original) The method according to claim 15, wherein said load
2 comprises a charge pump circuit for a phase-locked loop.

1 17. (Currently Amended) The method according to claim 15, wherein said
2 current mirror comprises at least three output ~~load~~ current source legs.

1 18. (Original) The method according to claim 17, wherein said current
2 mirror comprises at least three compensation devices plus the very first sensing
3 compensation device to compensate for gate current leakage in said all legs containing a
4 P-type CMOS transistor.

1 19. (Original) The method according to claim 18, wherein said
2 compensation devices comprise P-type CMOS transistors.

1 20. (Currently Amended) The method according to claim 19, wherein said
2 three output current ~~mirror~~ source legs each comprise at least one P-type CMOS
3 transistor and said three current compensation devices each provide compensation for all
4 of said P-type CMOS transistors.